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NASA CASE NO. NPO-17233-1CU

PRINT FIG. 1

NOTICE

198.

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NRO-JPL

POWER SUPPLY CONDITIONING CIRCUIT

Inventors: Lori E. Primas
Rohan C. Loveland
Contractor: Jet Propulsion Laboratory

JPL Case No. 17233
NASA Case No. NPO-17233-1-CU
Date: July 8, 1988

AWARDS ABSTRACT

A primary object of the invention is to utilize a DC input voltage having periodic and random deviations (PARD) and substantially remove the PARD in an output voltage which can then be used as a reference.

In Fig. 1, a conditioning circuit 10 includes a constant current diode D_1 with a high dynamic impedance which receives an input voltage with PARD or a deviation e_i. A zener diode D_2 with a low dynamic impedance is fixed in series with the constant current diode D_1 to form a voltage divider. This provides an output voltage with a deviation e_o which is substantially less than e_i. Fig. 2 shows a field effect transistor (FET) circuit 20 having the conditioning circuit 10 in conjunction with an operational amplifier U_1 and transistor Q to increase a current being produced by only the conditioning circuit 10. Fig. 3 shows the FET circuit 20 in series to thereby increase the rejection of PARD beyond that achieved by a single FET circuit 20. Small signal analysis of the circuit 20 (Figs. 4 and 5) indicates that the rejection of PARD is largely determined by the dynamic impedances of the diodes D_1, D_2 and the transconductance and resistance of the transistor Q_1. The number of constant current diodes D_1 and zener diodes D_2 can be varied according to specific needs, as shown, for example, in Fig. 6.

The novelty appears to lie in the use of a constant current diode in series with a zener diode with a large dynamic impedance between them. PARD on DC voltage inputs can be reduced sufficiently to permit the use of DC outputs on highly sensitive equipment.

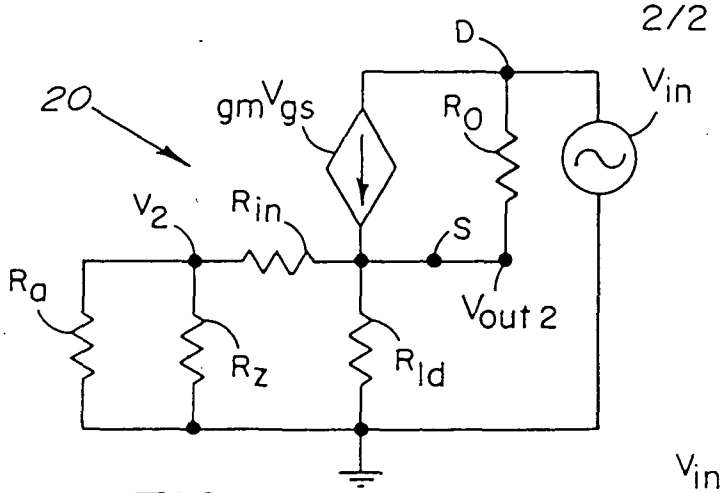


FIG. 5a

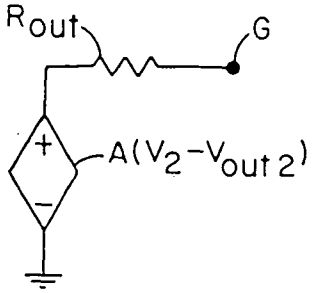


FIG. 5b

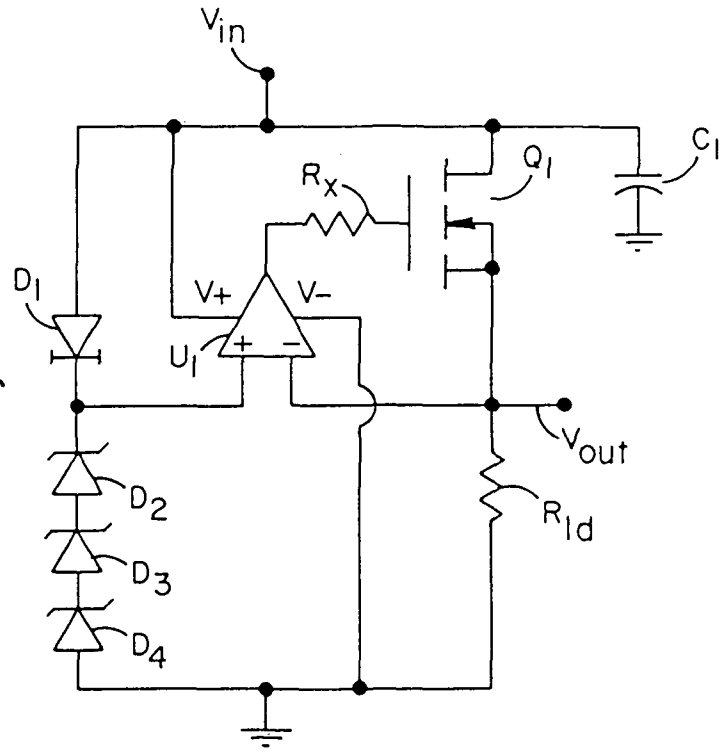


FIG. 6

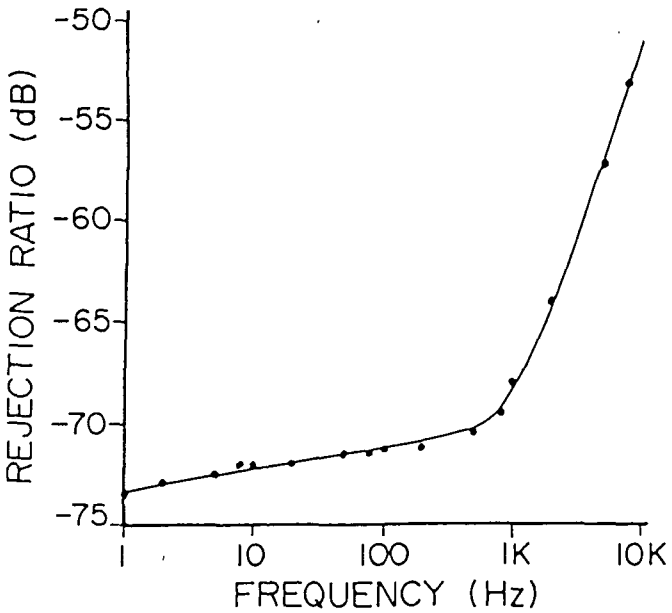


FIG. 7

JPL Case No. 17233
NASA Case No. NPO-17233-1-CU
Attorney Docket No. JPL1-N45

PATENT

Serial No. 231,025
Filing Date 8/11/88
Contract No. NAS7-918
Contractor Caltech/JPL
Pasadena (City) CA. (State) 91109 (Zip)

POWER SUPPLY CONDITIONING CIRCUIT

Origin of the Invention

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected not to retain title.

Technical Field

The present invention generally relates to a power supply conditioning circuit and, more specifically, to a circuit that can reduce periodic and random deviations on the output voltages of DC power supplies.

Background Art

DC power supplies are often characterized by the PARD on their output voltages. PARD is the periodic and random deviation of a DC voltage or current from its average value, over a specified bandwidth, with all influence and control quantities maintained constant. A bandwidth commonly used to specify PARD is 20 Hz to 20 MHz. PARD for a typical commercial low noise power supply is -74 dBV (200 microvolts/$(Hz)^{1/2}$) for frequencies above 20 Hz and is often much worse at frequencies below 20 Hz.

PARD on the output voltage of a power supply used to power RF circuitry results in undesirable AM and PM modulation of the RF signal being processed or generated. This problem is especially significant when using ultrastable frequencies generated by modern atomic frequency standards (e.g., σy (100 seconds) = 8.5 x 10^{-13} for cesium). To minimize the spurious AM and PM modulation of ultrastable frequencies, the PARD on the associated power supply voltages must be minimized. Most commercial power supplies do not reduce the periodic variations, which are predominately at 60 Hz and its harmonics, to a low enough level for use in ultrastable RF circuitry. These periodic variations should be reduced below the level of random deviation (noise). If phase noise of a low noise voltage-controlled oscillator exceeds the specification for spurious signals, PARD from the power supply might modulate the RF output signal.

Also, sidebands that are generated in frequency multiplier circuits as a result of PARD on the power supply voltage are of particular concern because the power in sidebands P_{sb} is increased by:

$$P_{sb} = 20 \log (f_2/f_1) \qquad (1)$$

where f_1 is the input frequency and f_2 is the output frequency of the multiplier. For example, if a 5 MHz reference frequency is multiplied to 10 GHz, the sidebands will increase by 66 dB. This increase in sideband power will often degrade the stability of the desired high frequency signal to an unacceptable level.

An attempt to reduce PARD is shown in U.S. Patent No. 4,667,279. Therein, an input of a high pass filter is coupled to the output circuit of the supply to receive a noise signal. The output of the high pass filter is coupled to a transformer via an amplifier, while the

FIG. 1

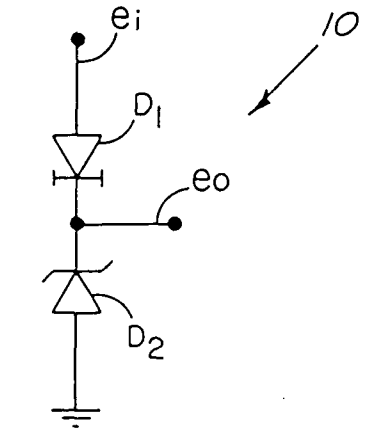


FIG. 2

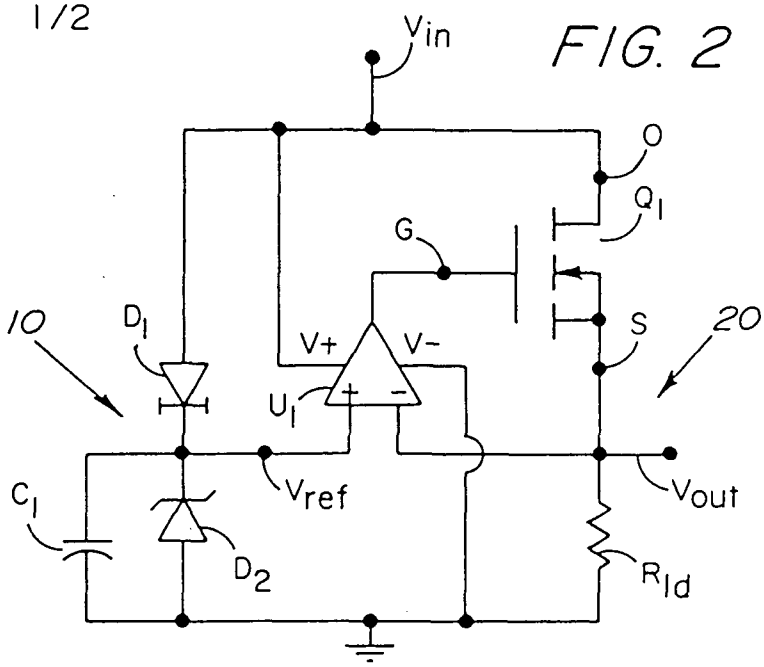
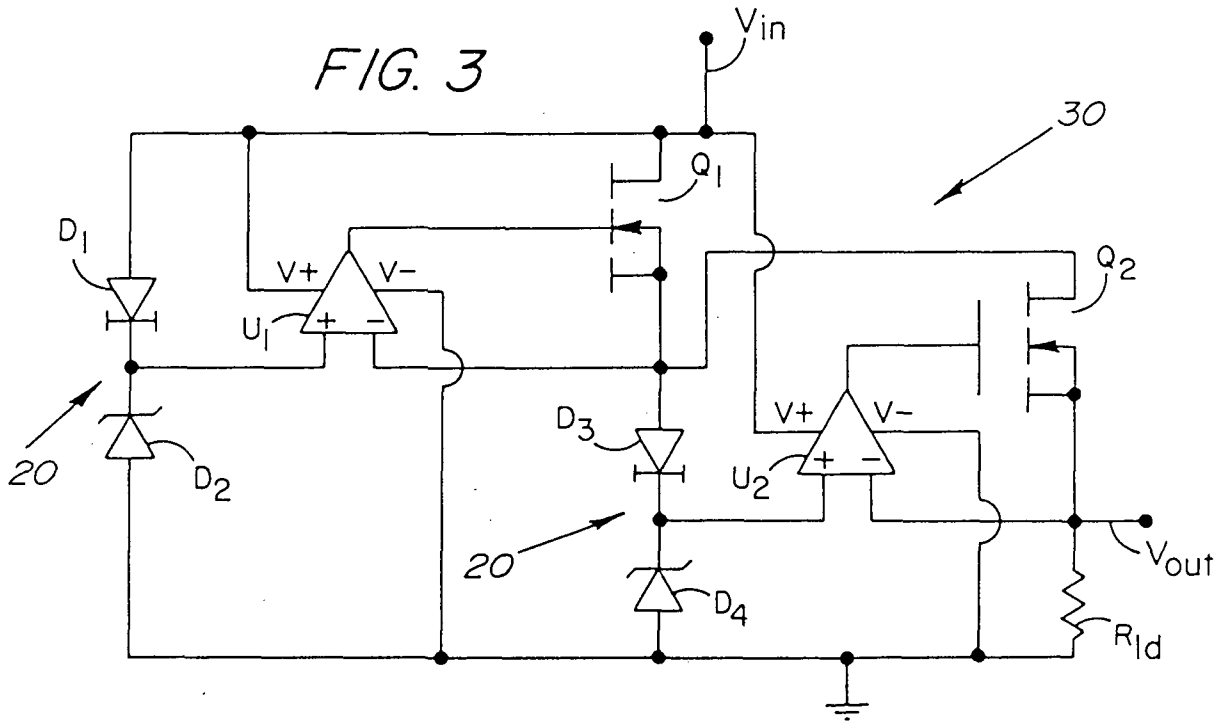


FIG. 3



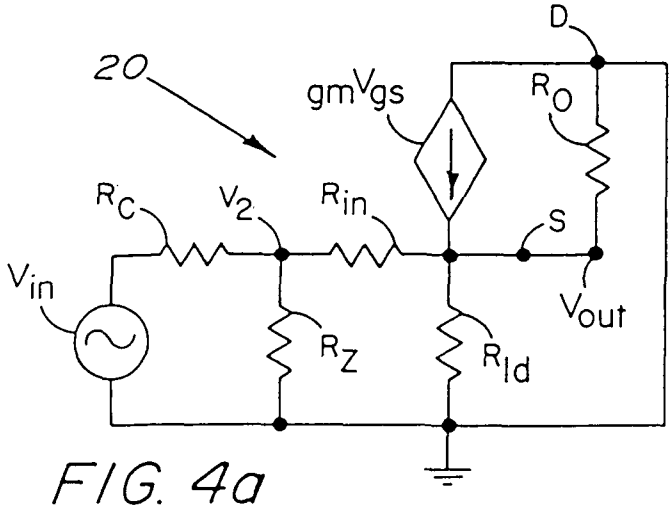


FIG. 4a

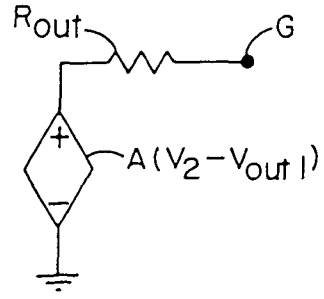


FIG. 4b

transformer is also coupled to the output of the supply. Another type of filtering is shown in U.S. Patent No. 4,594,648. A voltage sensing circuit between the output and common terminals of a filter produces a sense signal which is proportional to the output voltage at the output terminal. An amplifier receives the sense signal and generates a correction signal. The correction signal has a magnitude and waveform such that coupling the correction signal onto the output terminal of the filter eliminates or reduces the ripple and noise.

While the above do provide some PARD reduction, they still have drawbacks. For example, they do not provide DC power regulation and their range of rejected voltage is limited.

A need therefore still exists in the art for an improved circuit that effectively and significantly reduces PARD.

Statement of the Invention

Accordingly, it is an object of the present invention to provide an improved power supply conditioning circuit.

Another object of the present invention is to provide a circuit to reduce PARD on output voltages of DC power supplies.

Yet another object of the present invention is to reduce PARD to a level sufficient for circuitry involving ultrastable frequencies.

Still another object of the present invention is to reduce PARD while increasing a current output.

The objects of the present invention are particularly accomplished by utilizing large differences in the dynamic impedances of a constant current diode and a zener diode to establish a DC voltage with low PARD.

The above objects and others of the present invention can best be seen from an examination of the specification, claims and drawings hereto.

Brief Description of the Drawings

Fig. 1 is a schematic of a voltage reference circuit or conditioning circuit for low PARD according to the present invention;

Fig. 2 is a schematic of a field effect transistor (FET) circuit utilizing the conditioning circuit according to the present invention;

Fig. 3 is a schematic of a two-staged FET circuit utilizing the conditioning circuit according to the present invention;

Fig. 4 is a schematic of a small signal model with AC source on anode of a constant current diode of the present invention, wherein Fig. 4a shows voltage effects from a transistor in an FET circuit and Fig. 4b shows voltage effects for an operational amplifier in an FET circuit;

Fig. 5 is a schematic of a small signal model with AC source on the drain of an FET circuit according to the present invention, wherein Fig. 5a shows voltage effects from a transistor in an FET circuit and Fig. 5b shows voltage effects for an operational amplifier in an FET circuit;

Fig. 6 is a schematic of another example FET circuit utilizing the conditioning circuit according to the present invention; and

Fig. 7 is a graph of rejection ratio versus frequency for an FET circuit according to the present invention.

Detailed Description of the Invention

The following description is to enable any person skilled in the art to which the present invention pertains, or with which it is most nearly connected, to make and use the same, and sets forth the best mode contemplated by the inventors of carrying out their invention.

In Fig. 1, a conditioning circuit 10 according to the present invention is shown. The circuit 10 is capable of providing a DC reference voltage having extremely low PARD for frequencies ranging from DC to several KHz. Preferably, the circuit 10 can reduce PARD on the output voltage of a DC power supply (not shown) to -150 dBV (32 nanovolts per $(Hz)^{1/2}$).

In the circuit 10, a constant current diode D_1 and a zener diode D_2 in series form a voltage divider having a very large division ratio for AC signals. Using a standard voltage divider equation, a deviation e_o of an output voltage caused by a deviation in an input voltage e_i will be:

$$e_o = \frac{r_z}{r_c + r_z} e_i \qquad (2)$$

where

r_z = dynamic impedance of the zener diode, and

r_c = dynamic impedance of the constant current diode.

In a preferred embodiment, the dynamic impedance of the constant current diode D_1 can be greater than about 100K ohms and the dynamic impedance of the zener

diode D_2 can be less than about 10 ohms. If equation (1) is evaluated under the conditions that r_c = 100K ohms and r_z = 10 ohms, a rejection ratio e_o/e_i will be about 10^{-4} or -80 dB. Thus, the large dynamic impedance of the constant current diode D_1 and the small dynamic impedance of the zener diode D_2 cause deviation of the DC voltage applied to the input of the voltage reference circuit 10 to be greatly reduced at the output of the circuit 10.

As can be appreciated from the above example, the circuit 10 preferably uses a constant current diode D_1 with the highest possible dynamic impedance and a zener diode D_1 with the lowest possible dynamic impedance. However, certain compromises must then be made. Generally, the dynamic impedances of constant current diodes have an inverse relationship to the current rating. As the current ratings of constant current diodes go down, the dynamic impedances go up. As to the zener diode, it is preferable to use one which is designed to have a low impedance at a low current so that the highest possible impedance ratio consistent with good zener regulation can be obtained. Low voltage avalanche zener diodes can meet this requirement and have low noise as well.

Since the present invention achieves a maximum rejection ratio by the use of the lowest possible current, the circuit 10 is used as a voltage reference. However, to overcome low current output, the embodiments of the present invention described below use additional circuitry to maintain an output voltage with low PARD and also to increase the output current.

In a field effect transistor (FET) circuit 20 shown in Fig. 2, the reference circuit 10 is reproduced at the output using feedback. An operational amplifier U_1, used in conjunction with a field effect transistor Q_1,

increases the current capability. From an input voltage V_{in}, the diodes D_1, D_2 provide a reference voltage V_{ref} that is applied to the op amp U_1. An output voltage of the op amp U_1 controls the current through the transistor Q_1 in such a manner as to reproduce the reference voltage V_{ref} at a circuit output V_{out}. A load resistance R_{ld} represents a resistance on the drain voltage V_{out}, while a bypass capacitor C_1 keeps impedance of the zener diode D_2 low at high frequencies. Fluctuations on the drain voltage V_{out} are not reproduced at the source V_{ref} due to the high impedance between the drain and source.

For many applications, the rejection ratio provided by the circuit 20 is sufficient. If even more rejection is required, the rejection ratio can be increased by connecting two circuit 20 stages in series to provide a circuit 30, as shown in Fig. 3. In such an arrangement, a constant current diode D_1 with a zener diode D_2 operate vis-a-vis an operational amplifier U_1 and a field effect transistor Q_1. The transistor Q_1, however, can be readily omitted since, as apparent from the description below, current gain is then not necessary. Similarly, a constant current diode D_3 with a zener diode D_4 operate vis-a-vis an operational amplifier U_2 and a field effect transistor Q_2. In comparison to the circuit 20, the circuit 30 increases the rejection ratio by the square of the rejection ratio.

Referring to Figs. 4 and 5, a theoretical rejection ratio for the FET circuit 20 can be determined using a small signal analysis model. This analysis illustrates which parameters limit the performance of the circuit 20. Input PARD is represented by an AC voltage source V_{in}. Superposition may be used to determine the effect of the source V_{in} by applying the source V_{in} to different points in the model. In this particular case, the AC

source V_{in} is first applied to the anode of the constant current diode (Fig. 4) and then to the drain of the FET Q_1 (Fig. 5). In so doing, the effects of the source V_{in} are separated. Fig. 4 generally represents effects of V_{in} vis-a-vis diodes D_1, D_2. Fig. 5 represents the effects of V_{in} vis-a-vis the op amp U_1 and transistor Q_1.

Specifically, Fig. 4a shows a resistance R_c of the constant current diode D_1 and a resistance R_z of the zener diode D_2. V_2 represents the reference voltage produced by the diodes D_1, D_2. R_{in} is the input resistance to the op amp U_1. A gain and impedance of the transistor Q_1 is denoted $g_m Vgs$, while a resistance thereof is denoted R_o. Again, R_{ld} is the resistance on the drain. The letter S denotes the source voltage and D denotes a drain voltage, while V_{out_1} is an output voltage. Fig. 4b shows a gain A (V_2-V_{out}) produced by the op amp U_1 through its resistance R_{out}, and which produces a voltage G at a gate of the transistor Q_1.

Figs. 5a, b show a similar analysis as Figs. 4a, b, respectively, except that the AC source is moved to the drain side of the circuit 20.

The rejection ratios can be defined with standard equations in dB as follows:

$$Rr_1 = 20 \log \left[\frac{V_{out_2}}{V_{in}}\right], \text{ and} \quad (3)$$

$$Rr_2 = 20 \log \left[\frac{V_{out_2}}{V_{in}}\right], \text{ and} \quad (4)$$

$$Rr = 20 \log \left[10\exp\left(\frac{Rr_1}{20}\right) + 10\exp\left(\frac{Rr_2}{20}\right)\right] \quad (5)$$

where

Rr_1 = rejection ratio with the AC source connected to the anode of the constant current diode;

Rr_2 = rejection ratio with the AC source connected to the drain of the FET;

Rr_t = total rejection ratio;

V_{out_1} = AC output voltage with the AC source connected to the anode of the constant current diode;

V_{out_2} = AC output voltage with the AC source connected to the drain of the FET; and

V_{in} = AC input voltage.

As shown in equation (5), the overall rejection ratio of this circuit 20 is approximately equal to the poorer of the two independent rejection ratios.

For purposes of analysis, the FET circuit 20 was simplified by removing the bypass capacitor C_1. An analysis of the model with the AC source connected to the anode of the constant current diode (Fig. 4) shows the rejection ratio to be largely determined by the dynamic impedances of the constant current diode D_1 and the zener diode D_2. Using established principles, this is shown through the following equations which may be arrived at from the model:

$$\frac{V_2 - V_{in}}{R_c} + \frac{V_2}{R_z} + \frac{V_2 - V_{out_1}}{R_{in}} = 0 \qquad (6)$$

$$\frac{V_{out_1} - V_2}{R_{in}} = g_m Vgs - \frac{V_{out_1}}{R_{eq}} \quad (7)$$

$$Vg = A(V_2 - V_{out_1}) \quad (8)$$

$$Vs = V_{out_1} \quad (9)$$

$$Vgs = AV_2 - (A + 1)V_{out_1} \quad (10)$$

where

R_{in} = input impedance of operational amplifier

R_{out} = output impedance of operational amplifier

A = gain of operational amplifier

R_{eq} = $R_{ld}//R_o$

R_{ld} = load resistance

R_o = drain source resistance

Vg = AC gate voltage

Vs = AC source voltage

Vgs = AC gate to source voltage

g_m = transconductance of the MOSFET

Combining equations (6), (7), and (10) leads to:

$$\frac{V_{out_1}}{V_{in}} = \frac{R_{eq}(R_c//R_z//R_{in})(1 + g_m A R_{in})}{R_c[R_{eq} + R_{in} + g_m R_{in} R_{eq}(A + 1) - (1/R_{in} + g_m A)R_{eq}(R_c//R_z//R_{in})]} \quad (11)$$

With the assumptions

$$A >> 1$$

$$R_c >> R_z$$

$$R_{in} >> R_z$$

$$R_o >> R_{ld}$$

equation (11) reduces to

$$\frac{V_{out_1}}{V_{in}} = \frac{R_z}{R_c} \tag{12}$$

An analysis of the model (Fig. 5) with the AC source connected to the drain of the MOSFET (Q_1 in Fig. 2) shows this rejection ratio to be largely determined by the transconductance and drain to source resistance of the MOSFET Q_1, and the gain of the op amp U_1 (Equation 19 below). Using established principles, the following equations may be derived from the model:

$$\frac{V_{out_2}}{R_{ld}} + \frac{V_{out_2}}{(R_c//R_z) + R_{in}} = g_m Vgs + \frac{V_{in} - V_{out_2}}{R_o} \tag{13}$$

$$\frac{V_2}{R_c} + \frac{V_2}{R_z} = \frac{V_{out_2} - V_2}{R_{in}} \tag{14}$$

$$Vg = A(V_2 - V_{out_2}) \tag{15}$$

$$Vs = V_{out_2} \tag{16}$$

$$Vgs = AV_2 - (A + 1)V_{out_2} \tag{17}$$

Combining equations (13), (14), and (17) leads to

$$\frac{V_{out_2}}{V_{in}} = \frac{1/R_o}{\frac{1}{R_{ld}} + \frac{1}{(R_c//R_z)+R_{in}} + \frac{1}{R_o} + g_m(A+1) - \frac{g_m A(R_c//R_z//R_{in})}{R_{in}}} \quad (18)$$

With the assumptions

$A >> 1$

$R_c >> R_z$

$R_{in} >> R_z$

$R_o >> 1$

$R_{ld} > 1$

equation (18) reduces to

$$\frac{V_{out_2}}{V_{in}} = \frac{1}{g_m A R_o} \quad (19)$$

A component listing for an FET circuit 40 (Fig. 6) that incorporates the conditioning circuit 10 of the present invention and which was tested is given below:

D_1	1N5314	4.7 mA constant current diode
D_2, D_3, D_4	LVA351A	5.1V zener diode
U_1	OP-27	Low noise precision op amp (PMI)
Q_1	VN88AF	N-channel enhancement MOSFET
R_x		1K ohm resistor
R_{ld}		30 ohm resistor
C_1		1uF capacitor

The rejection ratio of this circuit 40 was determined by adding an AC voltage to the DC supply, and measuring the AC voltage present at the output V_{out} of the power supply conditioner. A -10 dBV AC signal was added to the input V_{in} and rejection ratios near -70 dB were measured for frequencies ranging from 1 Hz to 10 kHz. This is shown graphically in Fig. 7. The input voltage was 22.0V and the output voltage 15.3V, with an output current of 0.5A.

Equations (12) and (19) were used to compare the above experiential results (Fig. 7) with the theoretical results, using the following values:

$A = 10^6$

$g_m = 195 \times 10^{-3}$ siemens

$R_o = 3K$ ohms

$R_c = 50K$ ohms

$R_z = 15$ ohms

The theoretical rejection ratio due to the constant current diode and the zener diode is -70 dB, while that due to the MOSFET is -175 dB. Thus, in this case, the dynamic impedances of the constant current and zener diodes limit the rejection ratio to -70 dB.

As can be appreciated, the present invention contemplates the use of multiple zener diodes which can be selected to provide a specific impedance and resulting voltage. Similarly, multiple constant current diodes can be used, for example, to increase current from the reference.

The power supply conditioner described above provides a simple and effective way to reduce the PARD found on the output voltages of AC and DC power supplies. A low noise voltage reference, consisting of a

constant current diode and a low noise zener diode connected in series, provides the basis for this design. The rejection ratio of this design is determined by the ratio of the dynamic impedances of the constant current diode and the zener diode, and can be improved by increasing this ratio and using lower noise zener diodes. Further improvements can be made by connecting two stages in series. An additional advantage of this power supply conditioner is that it provides large current capabilities, making it a practical addition to systems requiring power supplies with low PARD down to DC.

The specifications above describe only preferred embodiments of the present invention, and it is contemplated that various modifications to the above can be effected but nevertheless come within the scope of the invention as defined by the claims.

POWER SUPPLY CONDITIONING CIRCUIT

ABSTRACT

A conditioning circuit is provided with a constant current diode in series with a zener diode, the former having a high dynamic impedance and the latter a low dynamic impedance. The constant current diode can receive an input voltage with PARD. In conjunction with the zener diode fixed to a ground, a voltage divider is provided which can give an output voltage whose PARD has been significantly reduced. The conditioning circuit is effective down to DC.